

Fig. 5: Flow chart describing the RR programming algorithm.

bitcell failure rate of a macro determines the total number of redundant sets required, and this technique can be added to protect any standalone SRAM macro in a digital design. BB adds a timing overhead of two multiplexers to the read delay. BB also requires a large write address setup time, but this overhead is not on the critical path.

The minimum operating voltage is limited by a few multi-bit faults, instead of an overwhelming number of single-bit faults. While BB can repair multi-bit failures in the tag arrays, DCR can only repair single-bit failures in the data arrays. At V_{DD} where the first double-bit failure appears in a cache set, DCR is correcting less than 1% of the sets. Line disable [3] is added to prevent accesses to lines with multi-bit failures, which allows DCR correction to be better utilized. Disable bits are stored with each tag, and the way-replacement algorithm avoids refills to disabled ways. Also, BB overhead could be reduced by using LD to also disable ways with failing tag bits.

The BIST detects SRAM error locations before operation, and uses the error information to program BB, DCR, and LD. To ensure redundancy is correctly programmed during every power-up, testing results either need to be stored in non-volatile memory, or retested and reprogrammed on every power-up. The flow chart in Figure 5 summarizes the RR programming algorithm. In this testchip, the BIST is run at a wide range of voltages and frequencies to identify V_{min} and the corresponding maximum frequency, while in a practical processor, existing binning techniques can be used to identify a smaller number of voltage and frequency points. While the fabricated prototype uses an off-chip programming loop for flexibility, an on-chip implementation could test the SRAM in around 20 ms for each voltage and frequency point.

Table I compares the resiliency, timing, and area overhead of the proposed technique compared to prior techniques for the L2 cache. The cited techniques do not disclose any resiliency or overhead results, so the comparison points are estimates. For this implementation of DCR, the data arrays are nominally 137 bits wide (128 bits plus 9 ECC check bits), and require 1 extra column for DCR plus small shifting logic. The nominal tag array width is 216 bits, and LD adds 8 bits while the RA for DCR adds an additional 13 bits (8 bits plus 5 ECC check bits). BB flip-flops and logic, implemented as standard cells, add about 15% to the tag macro area. However, the relative area of the tag portion of the L2 cache is only 6% of the total area, so the entire RR scheme adds only 2% area overhead to the L2 cache.

Technique	Maximum BER	Protects tags?	Area Overhead		Total Cache Overhead
			Tags	Data	
Proposed (BB+DCR+LD) §	9.8×10^{-5}	Yes	BB: 15% DCR: 6% LD: 4%	DCR: 0.7%	2.2%
Extreme Redundancy**	2.4×10^{-5}	Yes	SC: 6.4% Flops: 0.5%	SC: 6.4% Flops: 0.5%	6.6%
Line Disable § [3]	1.8×10^{-5}	No	4% #	-	0.2% #
ECC† [4]	1.3×10^{-6}	Yes	7% #	7%	6.7% #
Static Redundancy* [2]	4.4×10^{-7}	Yes	SC: 1% # Fuses: 0.12%	SC: 1% # Fuses: 0.12%	1.1% #
Nominal	1.1×10^{-10}	No	-	-	-

§ Up to 1% disabled **1 column repair/KB and 1 row repair/32KB

†1 repair/128 bit *10 repairs/MB

Estimate (not reported), fuse=100× bitcell, flop=10× bitcell

Note: Data portion is 90% of cache area, tag portion is 6% of cache area

TABLE I: Comparison of L2 cache area overhead and analytical estimates of allowable bitcell error rates for different techniques.

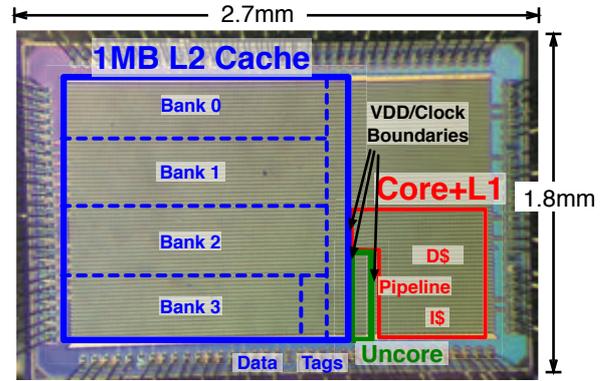


Fig. 6: Die micrograph with labeled processor core, L1 cache, and L2 cache.

Measurement Results

The single-core processor is fabricated in a TSMC 28nm HPM process with a 1.8 mm by 2.7 mm die area, as shown in Figure 6. The measured bitcell failure rate of the SRAM bitcells from a suite of March BIST tests is shown in Figure 7. The L1 cache is implemented with 8T-based bitcells, while the L2 cache is implemented with 6T-based bitcells. As expected, the 8T-based bitcells have a lower intrinsic V_{min} than the 6T cells, and the smaller absolute number of bits in the L1 provides less information about small bit error rates. The maximum allowable BER for the proposed technique and prior techniques from Table I is annotated on the figure.

A variety of benchmarks are run on the processor at different voltages and frequencies with RR disabled. Figure 8 shows the baseline shmoo for the L1 and L2 cache of 7 measured chips with the proposed resiliency features disabled.

To verify the V_{min} reduction enabled by RR and test the actual implementation, RR is programmed with the fault information at V_{min} , and the benchmarks are rerun at each voltage and frequency point. Figure 9 shows the measured V_{min} of the L2 cache for three options for seven evaluated chips: only line disable enabled, only DCR enabled, and a combination of DCR+LD. In all three cases, bit bypass is used to protect the tags, and less than 1% of cache lines are disabled. Enabling the RR techniques (BB and DCR+LD) decrease V_{min} by an average of 25% in the L2 cache.

The correction capability of ECC is not used in Figure 9 to decrease V_{min} , and ECC is used only to confirm that

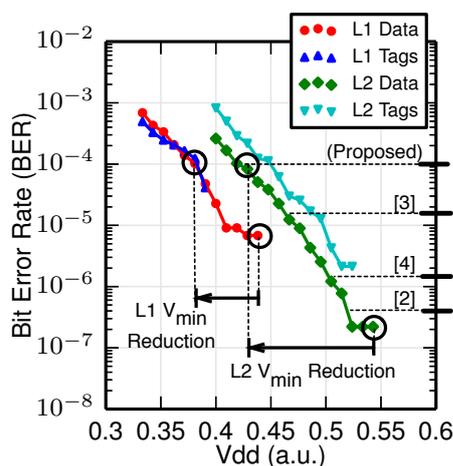


Fig. 7: Measured SRAM bitcell failure rate versus voltage for the L1 cache (6T bitcells) and L2 cache (8T bitcells).

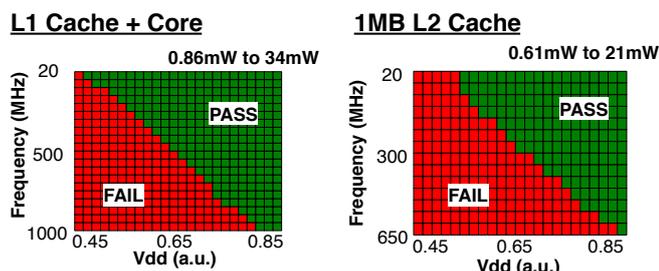


Fig. 8: Baseline L1 and L2 cache shmoo plot for benchmarks running on the processor without any of the reprogrammable redundancy techniques enabled.

all SRAM errors are identified during testing. Analysis of the SRAM failure maps predicts that using ECC correction alone would have achieved a 15% V_{min} reduction, but with a 7% area overhead. However, this result assumes that a BIST does not exist to identify the first double-bit failure, and V_{min} is limited by the worst array for a given yield target. By using BIST and setting a unique V_{min} for each chip, a 20% V_{min} reduction is possible. The 8T-based cells in the L1 already have excellent low-voltage performance for the tested chips, so RR decreases V_{min} in the processor as well, but only at voltages with extremely low frequencies that lie well below the energy-optimal point. In comparison to circuit techniques that report 130-200mV of V_{min} reduction for 5-7% area overhead [10], [11], the proposed RR techniques can achieve comparable effectiveness with less overhead. However, direct comparison is difficult as some reported modern bitcells are not designed to be used without SRAM assist, and the reported V_{min} reduction is optimistic. RR protects against all failure mechanisms, while circuit assist techniques must carefully tune assists to trade-off between different failure mechanisms.

Conclusion

The three proposed RR techniques, DCR, BB, and LD, reduce power in the L2 cache by 49% through improved supply voltage scaling with less than 2% area overhead and minimal timing overhead, and can be combined with existing assist techniques to enable further V_{min} reduction. Reprogrammable redundancy is particularly attractive because it can be used in conjunction with simple SECDED codes to protect against soft errors, and online reconfiguration based on ECC results or power-on tests can reduce voltage margin required for intermittent and aging-related faults.

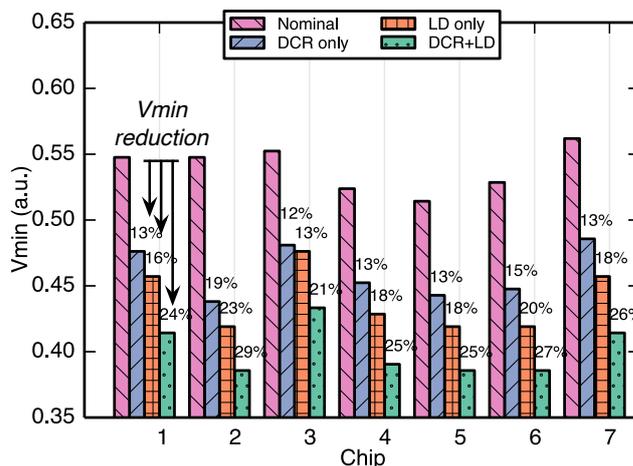


Fig. 9: Enabling the proposed reprogrammable redundancy reduces the minimum operating voltage of the L2 cache by 25%.

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