Agile Hardware Design: Building Chips with Small Teams

Yunsup Lee
ASPIRE Graduate 2016
Co-Founder and CTO
World’s First Single-Chip Microprocessor That Communicates Directly Using Light
Memory controller

50/50 Power Splitter

Transmitter

Receiver

RISC-V processor

1MB memory bank

Processor to memory link

Command + address + write data

Memory to processor link

read data

Optical amplifier

Laser

Single-mode fiber

Optical amplifier

Receiver

Transmitter

1MB memory bank (inactive)

RISC-V processor (inactive)

Electrical bus

Control FPGA
How did we build working microprocessors with such a small team?
more info for various components of the water cycle in climate prior to oil.
But there were the unknown unknowns along the way...
Wait, why are all outputs floating?
Dude, where's my Termination Resistor??

Output drivers not connected to pad!!!
Decoupling Caps are Too Far Away!
Agile Hardware Design

- Specification
- Design
- Implementation

- Big tape-out
- Small tape-out
- Tape-in
- ASIC flow
- FPGA
- C++
10+ Tapeouts at Berkeley
Enabling Small Teams to Build Custom Silicon
• We contribute to the open-source Freedom SoC platform based on RISC-V and open-source infrastructure
• We build customized Freedom SoCs as a service, which is quick, easy, and predictable at low upfront cost
Freedom Everywhere SoCs
Low power, 32-bit microcontrollers
Freedom E310

- First RISC-V based SoC based on the Freedom Everywhere SoC platform
- Target markets: IoT, Wearables, Embedded
- Low-power, low-cost, high-performance
- Open-source software and tools support
Freedom E310 Chip Block Diagram

First RISC-V SoC based on the Freedom Everywhere SoC platform

- 320+ MHz SiFive E31 CPU
- 1.61 DMIPS/MHz
- 16KB L1 I$
- 16KB Data Scratchpad
- Hardware Multiply/Divide
- Debug Module
- Multiple Power Domains
- Low Power Standby
- Wide Range of Clock Inputs
- TSMC180G
- 6mmx6mm 48-Pin QFN
Freedom E310 Chip

~6mm² in TSMC 180nm
HiFive1: Arduino-Compatible RISC-V Dev Kit
Powered by the Freedom E310 chip

- **Operating Voltage**: 3.3 V and 1.8 V
- **Input Voltage**: 5 V USB or 7-12 VDC Jack
- **IO Voltages**: Both 3.3 V or 5 V supported
- **Digital I/O Pins**: 19
- **PWM Pins**: 9
- **SPI Controllers/HW CS Pins**: 1/3
- **External Interrupt Pins**: 19
- **External Wakeup Pins**: 1
- **Flash Memory**: 128 Mbit Off-Chip (ISSI SPI Flash)
- **Host Interface (microUSB)**: Program, Debug, and Serial Communication

$59, https://www.crowdsupply.com/sifive/hifive1

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Freedom Unleashed SoCs

64-bit multi-core SoCs for embedded computing
Freedom U500 Base Platform Block Diagram

TSMC 28nm Chip for Rapid Customization of the Freedom Unleashed Platform

- U54-MC Coreplex
  - Single- and Double-precision floating-point support
  - Banked L2$ with directory-based cache-coherence
  - Modern OS support
- ChipLink
  - Serialized Chip-to-Chip TileLink Interconnect
- GbE
- Peripherals
- DDR3/4
Freedom U500 Base Platform Chip

~30mm$^2$ in TSMC 28nm

- 250M transistors
- 1.5 GHz+ SiFive E51/U54 CPU
  - 1x E51: 16KB L1I$ and 8KB DTIM
  - 4x U54: 32KB L1I$ and 32KB L1D$
  - ECC support
- Banked 2MB L2$
  - ECC support
- TSMC 28HPC
- FCBGA package
- Development board available in Q1 2018

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What’s Next?
Taking Agile Hardware Design to the Next Level

• Agile Verification: Did we build the thing right?
  • What role does Chisel/FIRRTL play?
  • Formal verification methodology on the horizon

• Agile Validation: Did we build the right thing?
  • On-demand FPGAs (e.g., Amazon F1) will play big role
  • High-fidelity emulation will become more important

• Agile Analog Design
  • How do we write portable Analog design?

• Enabling agile hardware design will spur innovation!