



Debugging BOOM-v2 with FPGA Simulation

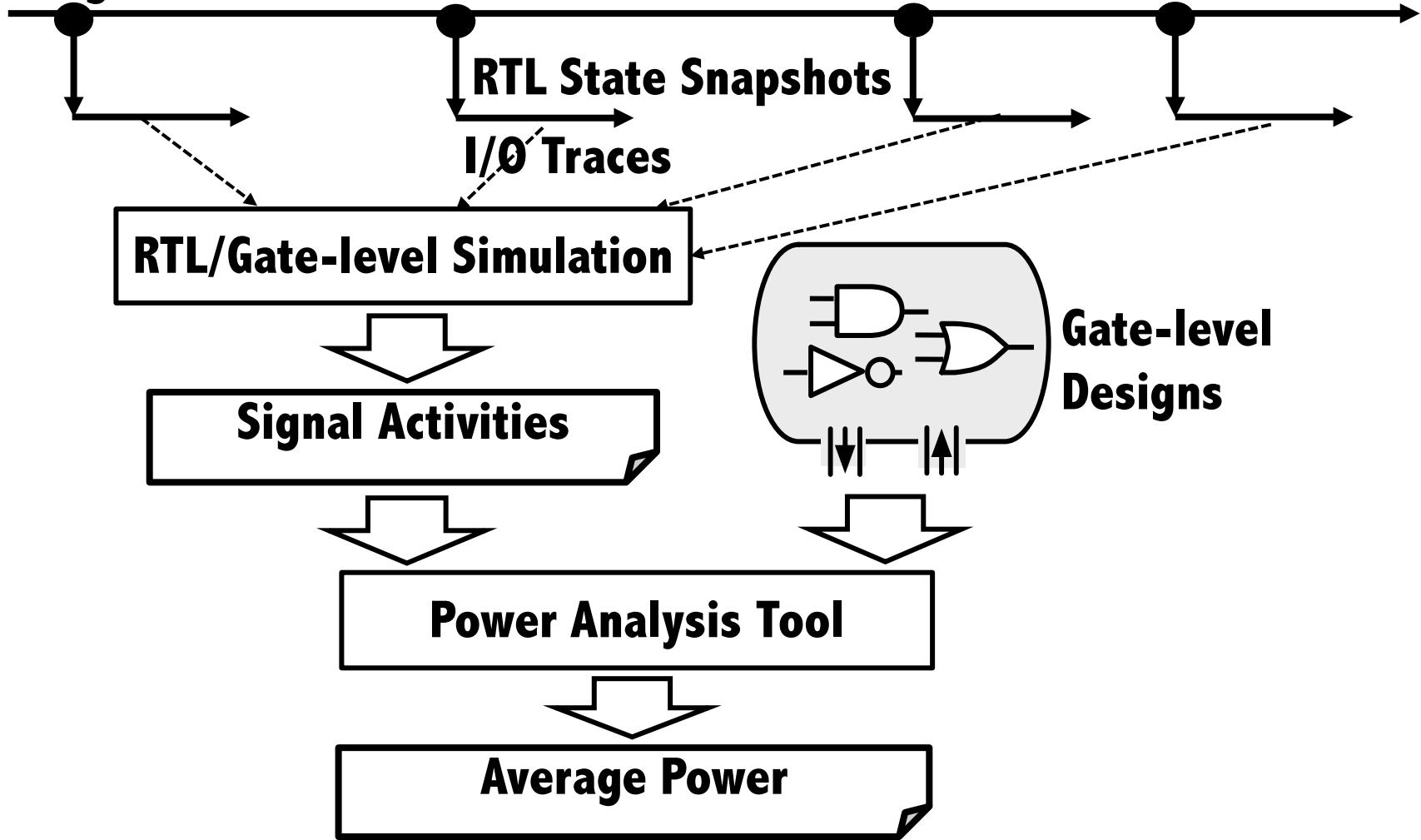
Donggyu Kim



Berkeley Architecture Research

ASPIRE End of Project Party
12/4/2017

Full Program Execution In FPGA



- Whenever we see this...

```
0016(P) 4888 0 28 36.445 40.777 42.342 0 0 FRM 0^M
0017(P) 4376 0 28 36.385 40.667 42.267 0 0 FRM 0^M
0018(P) 4016 0 28 36.517 40.733 42.220 0 0 FRM 2^M
0019(P) 3136 0 28 36.437 40.670 42.046 0 0 FRM 0^M
0020(P) 2936 0 28 36.389 40.680 41.964 0 0 FRM 0^M
0021(P) 3384 0 28 36.434 40.723 42.224 0 0 FRM 1^M
0022(P) 4240 0 28 36.615 40.538 42.228 0 0 FRM 1^M
0023(P) 3552 0 28 36.573 40.486 42.021 0 0 FRM 2^M
0024(P) 4096 0 28 36.659 40.447 42.110 0 0 FRM 1^M
0025(P) 3448 0 28 36.425 40.319 42.190 0 0 FRM 0^M
0026(P) 2872 0 28 36.417 40.338 42.381 0 0 FRM 1^M IITE has captured 0 stones^M
0027(P) 1696 0 28 36.440 40.363 42.345 0 0 FRM 0^M .ACK has captured 0 stones^M
0028(P) 1688 0 28 36.393 40.436 42.159 0 0 FRM 0^M
0029(P) 2120 0 28 36.416 40.550 42.106 0 0 FRM 0^M
0030(P) 2496 0 28 36.495 40.551 42.125 0 0 FRM 0^M
0031(P) 2888 0 28 36.545 40.552 42.030 0 0 FRM 1^M
0032(P) 3368 0 28 36.439 40.582 41.759 0 0 FRM 0^M
0033(P) 4184 0 28 36.487 40.705 41.853 0 0 FRM 2^M
0034(P) 3928 0 28 36.542 40.728 41.935 0 0 FRM 2^M
0035(P) 3904 0 28 36.548 40.690 42.265 0 0 FRM 1^M
0036(P) 3904 0 28 36.556 40.693 42.076 0 0 FRM 2^M
0037(P) 4008 0 28 36.529 40.652 42.098 0 0 FRM 3^M
0038(P) 3584 0 28 36.545 40.714 41.870 0 0 FRM 1^M
0039(P) 2832 0 28 36.630 40.692 41.900 0 0 FRM 0^M
0040(P) 2672 0 28 36.651 40.679 41.766 0 0 FRM 0^M
0041(P) 3512 0 28 36.718 40.652 41.669 0 0 FRM 4^M
0042(P) 358Illegal instruction^M
Segmentation fault^M
Setting Default Parameters...^M
Parsing Configfile sss_encoder_main.cfg.....
```

:o gnugo@gnu.org^M
above this message.^M



Chisel

Target RTL Design

FIRRTL Compiler

Assertion & Print Synthesis

FAME1 Transform

Scan Chain Insertion

Simulation Mapping

Platform Mapping

Verilog

FPGA Backend Flow

Bitstream / AFI Image

FPGA Simulation

- Assertion & Print Synthesis
 - Assertions and prints in FPGA
- FAME1 Transform
 - Accurate performance modeling in FPGA
 - Deterministic simulation with the same initial state
- Scan Chain Insertion
 - Initialize the target state
 - RTL state snapshot for error replays



Chisel

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Platform Mapping

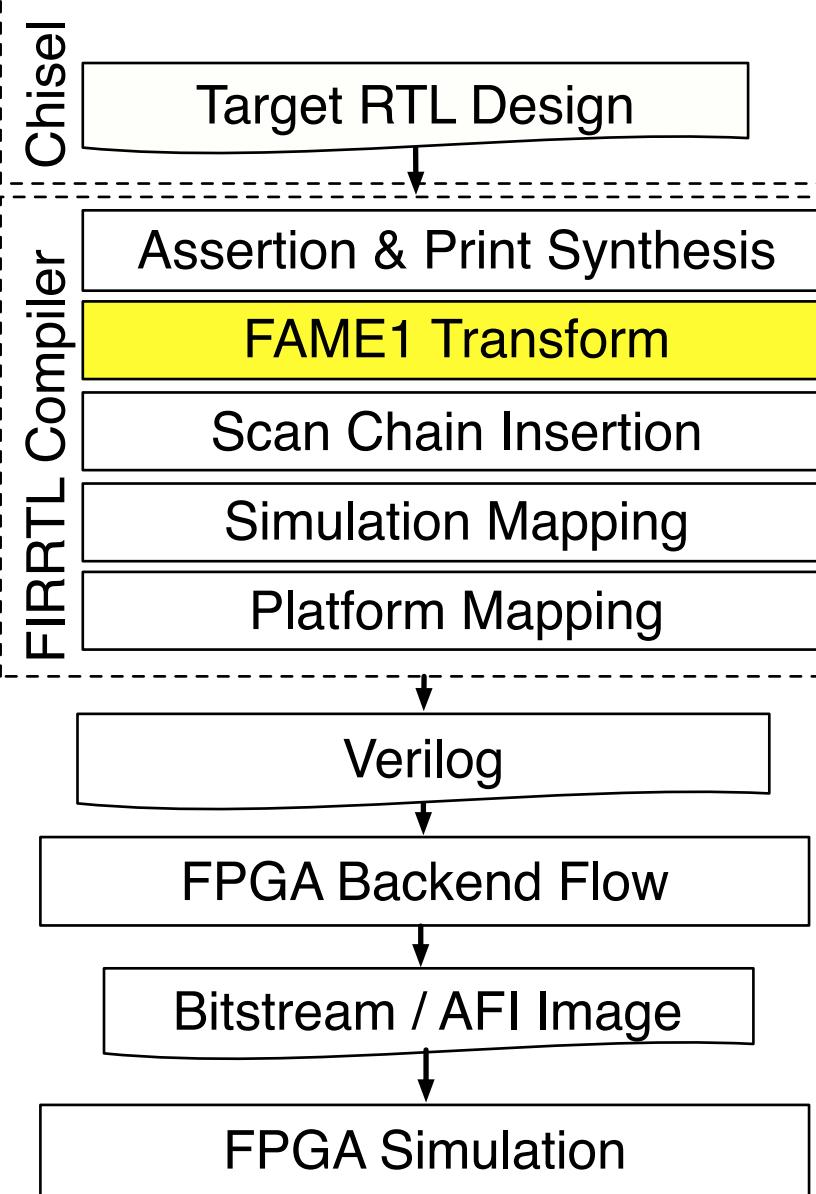
Verilog

FPGA Backend Flow

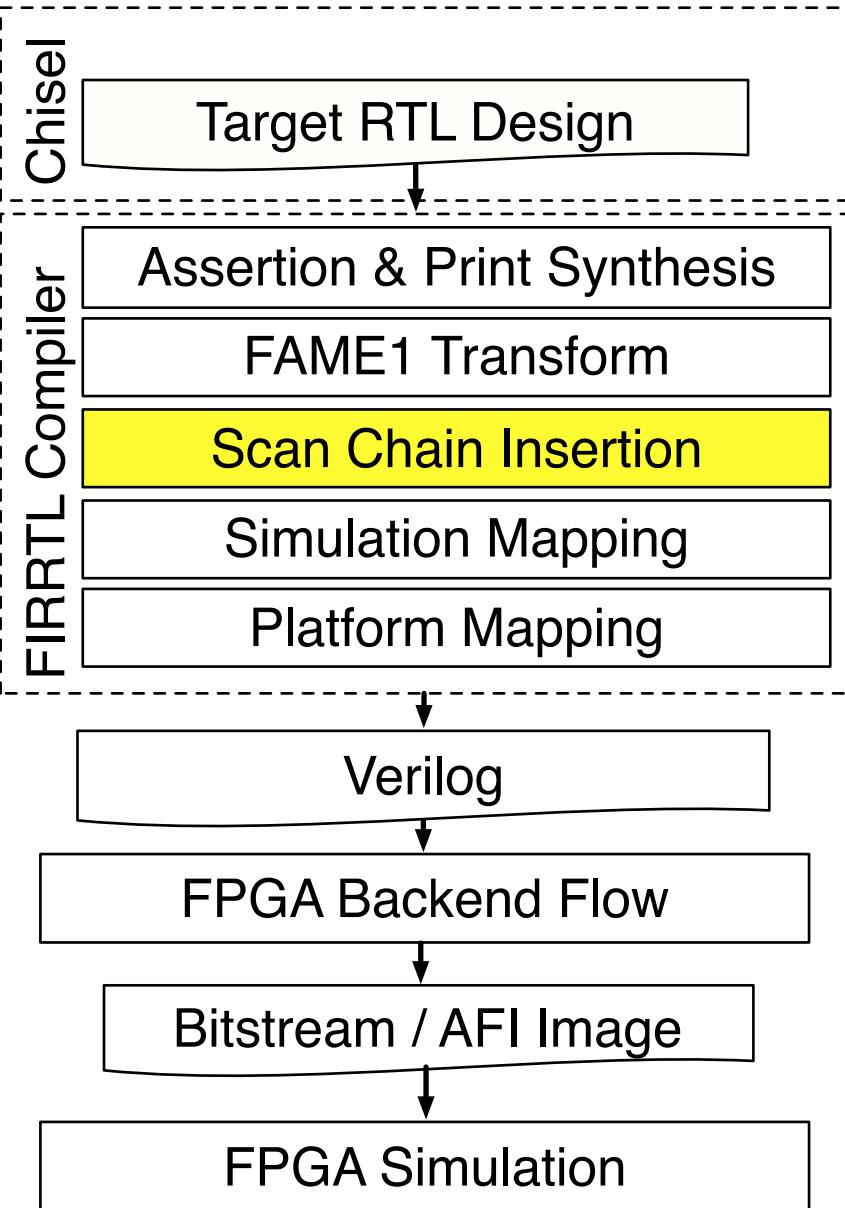
Bitstream / AFI Image

FPGA Simulation

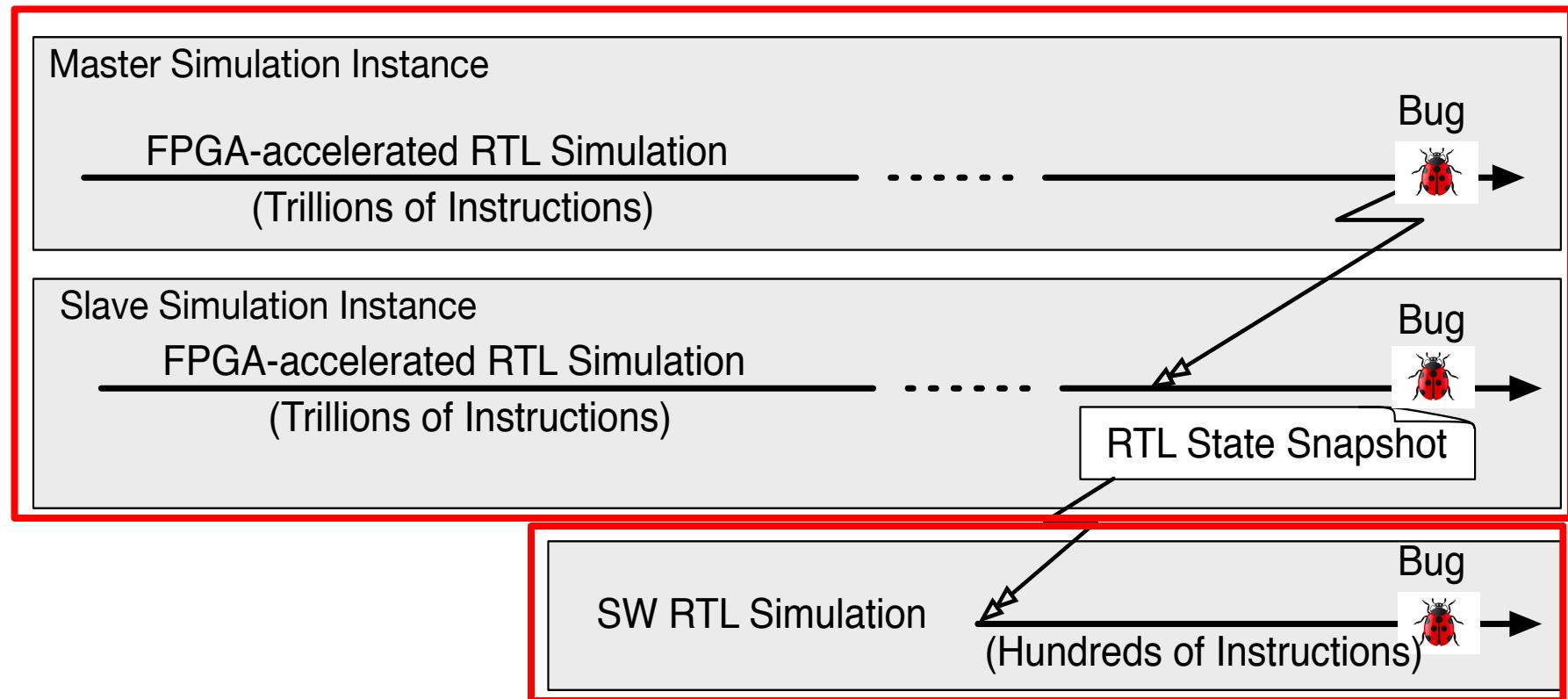
- **Assertion & Print Synthesis**
 - Assertions and prints in FPGA
- **FAME1 Transform**
 - Accurate performance modeling in FPGA
 - Deterministic simulation with the same initial state
- **Scan Chain Insertion**
 - Initialize the target state
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- Assertion & Print Synthesis
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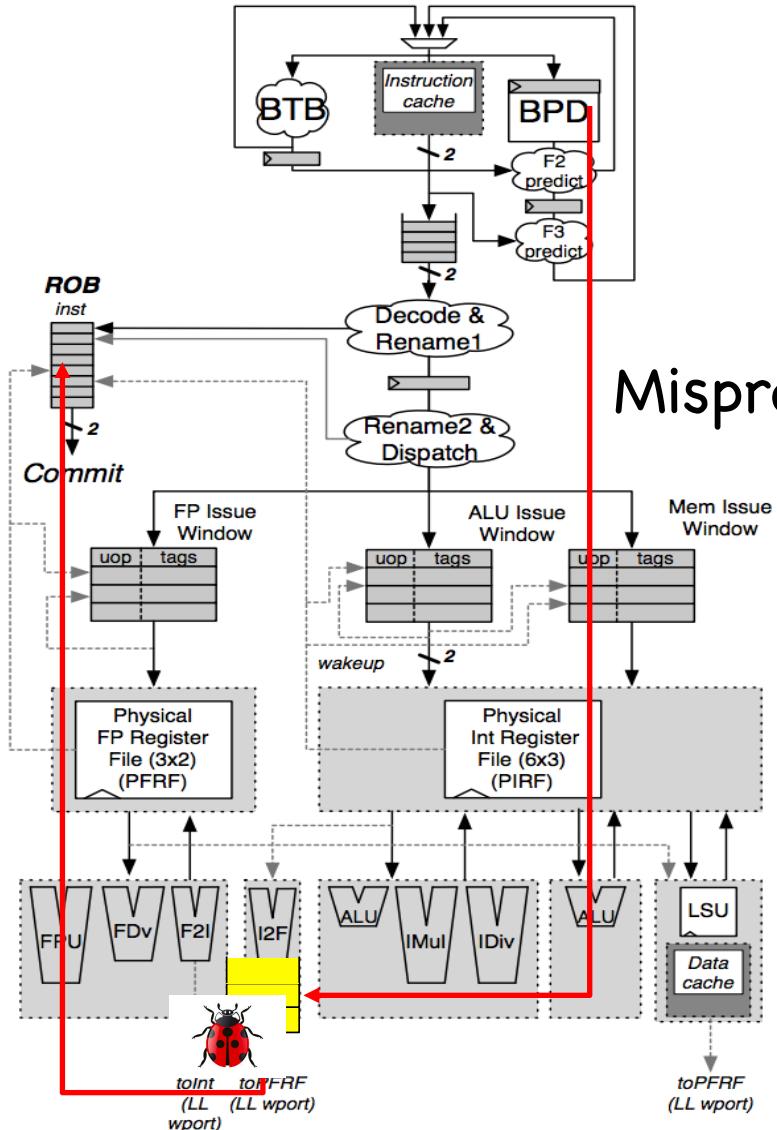


- *Master* catches errors from assertion
- *Slave* takes an RTL state snapshot for replays
- *Software simulation* replays the RTL snapshot for full visibility

Where Is the Bug?



Roll back
Wrong Data





This Bug was Fixed!



[util] Fix bug in FPtoInt queue.

* Bad copy/paste of flow-through queue causes valid to be set even for entries killed by a branch misspeculation.

h/t @donggyukim.

master v2.0.1

ccelio committed on Sep 11

1 parent d4688c5 commit 507491954c9423bdb16bfba5a89ae558888a463

[Browse files](#)

Showing 1 changed file with 7 additions and 5 deletions.

[Unified](#) [Split](#)

12 src/main/scala/util.scala

[View](#)

```
@@ -44,7 +44,7 @@ object GetNewUopAndBrMask
44 44     def apply(uop: MicroOp, brinfo: BrResolutionInfo)(implicit p: config.Parameters): MicroOp =
45 45     {
46 46         val newuop = Wire(init = uop)
47 -     newuop.br_mask :=_
47 +     newuop.br_mask :=
48 48         Mux(brinfo.valid,
49 49             (uop.br_mask & ~brinfo.mask),
50 50             uop.br_mask)
@@ -278,6 +278,7 @@ object AgePriorityEncoder
278 278     }
279 279
280 280
281 282     +// Assumption: enq.valid only high if not killed by branch (so don't check IsKilled on io.enq).
282 282     class QueueForMicroOpWithData(entries: Tnt, dataWidth: Tnt)(implicit p: config.Parameters) extends RoomModule(1)(p)
```

BOOM-v2 Assertion Results



Benchmark	Assertion	Cycle(B)	Simulation Time (Min)
483.xalancbmk.test	Invalid write back in ROB	1.9	3.4
464.h264ref.test	Pipeline hung	3.2	3.8
471.omnetpp.test	Pipeline hung	3.3	3.9
445.gobmk.test	Invalid write back in ROB	14.9	9.0
471.omnetpp.ref	Pipeline hung	62.6	22.2
401.bzip2.ref	Wrong JAL target	473.7	164.6

- Cost: 2 x 50 cents / hour
- Total cost: \$2 (compilation) + 2 x \$1.56 (simulation) = \$5.12